

Quasi-Resonant DC-DC Converters with Reduced Body Diode Loss

FIELD OF THE INVENTION

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The present invention relates generally to electrical power supplies. More particularly, it relates to buck DC-DC converters having a resonant capacitor and resonant inductor that provide increased efficiency and reduced output voltage.

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BACKGROUND OF THE INVENTION

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Buck converters are commonly used in electronics for changing the voltage or polarity of a power supply. They are often used to provide low voltage, high current output power. Buck converters typically employ two electronic switches (typically MOSFETs) in combination with an output inductor. The switches are alternately turned on, thereby providing voltage pulses to the output inductor.

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During portions (dead times) of the switching cycle, both switches are off. When both switches are off, the output inductor produces freewheeling current that flows through the integral body diode of one of the switches. Body diode current produces substantial energy loss due to the forward-bias voltage drop across the diode, thereby reducing the energy efficiency of the buck converter. Additionally, reverse recovery loss occurs when the body diode later becomes reverse-biased. In order to improve the efficiency of buck converters, body diode conduction and reverse recovery losses must be reduced.

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In order to provide buck converters with small size and weight, and reduced cost, it is best to operate the buck converter at high frequency. However, energy loss from both body diode conduction and reverse recovery increase dramatically with increasing operating frequency. In this way, body diode conduction and reverse recovery tend to limit the maximum operating frequency of buck converters.

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Also, state of the art microprocessors and digital electronics require exceptionally low supply voltages at high current. In order to provide such electrical power from a fixed-voltage

DC supply, the power supply must have a greater voltage step-down ratio. However, a high voltage step-down ratio is typically accomplished by reducing the duty cycle of the buck switches, which tends to increase switching losses. The switching losses are also increased by high frequency operation.

5 Additionally, it is noted that conventional buck converters operate the switches in hard switching mode. That is, the switches are conducting current when they are turned off, and they have voltage applied when they are turned on. Hard switching results in large switching loss and reduced reliability of the switches. It would be an advance in the art of buck converter design to provide a buck converter that has soft switching or nearly-soft switching
10 (i.e. zero- or low-voltage at turn-on, and zero- or low-current at turn off).

 More generally, it would be an advance in the art of buck converter design to provide a buck converter having reduced switching loss, body diode current loss and soft switching. Such a buck converter could operate with very high efficiency compared to conventional buck converters, and could operate at high frequency. High frequency capability can provide many
15 benefits such as smaller size and weight, and reduced cost.

SUMMARY OF THE INVENTION

 The present invention includes a quasi-resonant buck converter having a top switch
20 and an auxiliary switch connected in series between a power source V_{in} and a return potential Gnd. A resonant inductor is connected to a connection point between the top and auxiliary switches. A synchronous switch and resonant capacitor are connected between the resonant inductor and the return potential.

 The operation of the synchronous switch can be phase shifted to control output power.
25 The OFF time of the synchronous switch is preferably approximately equal to a resonant period of the resonant inductor and resonant capacitor, $\frac{3}{2}\pi\sqrt{LC}$, where L is the inductance of the resonant inductor, and C is the capacitance of the resonant capacitor.

 In an alternative embodiment, the circuit has coupled inductors. The coupled inductors are connected in series and in series with the resonant inductor. The resonant capacitor and

synchronous switch are connected to a midpoint of the coupled inductors. In this embodiment, the coupled inductors tend to reduce output voltage, and thereby allow a greater duty cycle and consequently, provide reduced switching losses and greater efficiency.

In this embodiment the resonant period is given by $\frac{3}{2}\pi\sqrt{(L+L_k)C}$ where L is the inductance of the resonant inductor, L_k is the leakage inductance of the primary coupled inductor, and C is the capacitance of the resonant capacitor. Preferably, the resonant half-period is in the range of about 0.05 to 5 microseconds. Also preferably, the circuit is controlled so that an OFF time of the synchronous switch is approximately equal to $\frac{3}{2}\pi\sqrt{(L+L_k)C}$.

The circuit can also include a controller for controlling the operation of the switches so that output power or output voltage can be set to a certain value, or varied. Control over output power and output voltage is provided by timing the operation of the switches.

In another embodiment of the invention, an isolation transformer is provided between the resonant inductor and the synchronous switch and resonant capacitor. The isolation transformer provides isolation between the input and output of the circuit.

In this embodiment the resonant period is given by $\frac{3}{2}\pi\frac{N_s}{N_p}\sqrt{(L+L_k)C}$ where L is the inductance of the resonant inductor, L_k is the leakage inductance of the transformer, C is the capacitance of the resonant capacitor, N_s is the number of turns in the transformer secondary winding, and N_p is the number of turns in the transformer primary winding. Preferably, the resonant period is in the range of about 0.05 to 5 microseconds. Also preferably, the circuit is controlled so that an OFF time of the synchronous switch is approximately equal to the resonant period $\frac{3}{2}\pi\frac{N_s}{N_p}\sqrt{(L+L_k)C}$.

The transformer-isolated circuit can also include a controller for controlling the operation of the switches so that output power or output voltage can be set to a certain value, or varied. Control over output power and output voltage is provided by timing the operation of the switches.

DESCRIPTION OF THE FIGURES

Fig. 1 (Prior Art) shows a conventional buck converter according to the prior art.

Fig. 2 shows a quasi-resonant buck converter according to the present invention.

5 Fig. 3 shows a timing diagram illustrating operation of the circuit of Fig. 2.

Figs. 4A-4D illustrate circuit conditions during the four time periods A, B, C and D of Fig. 3.

Fig. 5 shows a quasi-resonant tap-buck converter according to the present invention.

10 Fig. 6 shows a timing diagram for operating the quasi-resonant tap-buck converter of Fig. 5.

Figs. 7A-7D illustrate circuit conditions for the circuit of Fig. 5 during the time periods A, B1, B2, C, and D of Fig. 6.

Fig. 8 shows a transformer-isolated quasi-resonant converter according to the present invention.

15 Fig. 9 shows a timing diagram for operating the circuit of Fig. 8.

Figs. 10A-10D illustrate circuit conditions for the circuit of Fig. 8 during time periods A, B1, B2, C, and D of Fig. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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The present invention provides a buck converter having a resonant capacitor and resonant inductor. In operation, the resonant capacitor and inductor apply voltage and current across the switches so that soft switching (or nearly-soft switching) is provided. Also, the resonant capacitor and resonant inductor help to transfer output power. Body diode current
25 loss is reduced in the present buck converters. Specifically, the resonant capacitor and resonant inductor apply a reverse current through the body diodes of the buck switches at turn-on so that zero-voltage switching (ZVS) is provided. Also, the resonant capacitor and inductor oppose current flow through buck switches at turn-off so that near-zero current switching (ZCS) is provided. Also, in one embodiment, a coupled inductor provides for

reduced output voltage even with relatively high duty cycle. Additionally, an isolated embodiment is provided.

Fig. 1 shows a buck converter according to the prior art. The buck converter has switches S1 S2 connected between Vin and Gnd. Gnd is the return potential for Vin; Gnd does not have to be Earth ground. An output inductor Lo and output capacitor Co provide filtering for the power provided to the load. In operation, both switches S1 and S2 experience hard switching at turn-on and turn-off, which produces switching loss. The switching loss increases rapidly with operating frequency. Additionally, during a dead time after S1 turn-off and before S1 turn-on, the body diode of S2 will conduct current due to the freewheeling output inductor Lo, resulting in energy loss and reverse recovery loss. The energy loss of S2 body diode current increases rapidly with operating frequency. These shortcomings render the device of Fig. 1 unpreferable for use in applications requiring high operating frequency, low output voltage and high output current.

Fig. 2 shows a quasi-resonant buck converter according to the present invention. The quasi-resonant buck of Fig. 2 has a top switch Q1 and an auxiliary switch Q2 connected across Vin and Gnd (Vin is positive in the specific embodiment shown). The top switch Q1 and auxiliary switch Q2 are connected at a connection point 20. A resonant inductor Lr is connected to the connection point. A resonant capacitor Cr is connected between the resonant inductor and Gnd. A synchronous switch Q3 is connected in parallel with the resonant capacitor Cr. An output inductor Lo and a Load are connected in series across the synchronous switch Q3. An output capacitor Co is connected in parallel with the Load.

Preferably, the switches Q1 Q2 Q3 are low on-resistance power MOSFETs or a similar kind of electronically controlled switch. The switches Q1 Q2 Q3 have gates (not shown) which are controlled by a gate controller (not shown) for turning the switches Q1 Q2 Q3 ON and OFF, as known in the art. Alternatively, switches Q1 Q2 Q3 can be insulated gate bipolar transistors (IGBTs) or bipolar transistors, which may be preferred in high voltage or high power applications.

The resonant inductor Lr and output inductor Lo may have magnetic cores made of ferrite, for example.

The load can be a microprocessor, digital electronics, communication electronics or any device that requires voltage lower than V_{in} .

The power supply V_{in} can be positive (as in Fig. 2) or negative.

Fig. 3 shows a timing diagram for operating the quasi-resonant buck converter of Fig. 2. Dark horizontal lines indicate when switches Q1 Q2 Q3 are ON. One full cycle of operation is divided into four time periods A B C and D. The durations of time periods A B C and D are not necessarily equal; the durations can be adjusted to provide a desired output power and output voltage, as explained below. The time period boundaries are indicated by transitions T1 T2 T3 T4. It is noted that at transitions T2 and T4 there will be a short (e.g. tens of nanoseconds or less) dead times so that switches Q1 and Q2 are never ON at the same time. Also illustrated in Fig. 3 are the voltage across the resonant capacitor C_r (V_{Cr}) and the current through inductor L_r (I_{Lr}).

Figs. 4A-4D illustrate circuit conditions during time periods A-D, respectively. Figs. 4A-4D are explained below. Arrows in the circuit illustrations indicate the direction of current flow. For brevity, the output capacitor C_o is not illustrated.

Fig. 4A (Time period A): Q1 and Q3 ON, and Q2 are OFF. Current from V_{in} rises linearly and charges resonant inductor L_r . Output inductor L_o is freewheeling. It is noted that essentially all of the energy supplied by V_{in} during time period A is stored in the resonant inductor L_r . It is also noted that the current through resonant inductor L_r should rise to a level greater (e.g. 10-100% greater) than the Load current I_{load} , illustrated in Fig. 3 by a horizontal line. Time period A is a charging period and so the duration of time period A determines the output power provided to the load. More specifically, the overlapping ON time of switches Q1 and Q3 determines the output power. In other words, increasing the duration of time period A increases the output power.

Fig. 4B (Time period B): Q1 is OFF, and Q2 and Q3 are ON. Resonant inductor L_r and output inductor L_o are both freewheeling. Freewheeling current from L_r flows through switches Q3 and Q2, but not into the Load. Current through L_r remains essentially constant. The current flowing through Q3 is equal to ΔI ($\Delta I = I_{Lr} - I_{Load}$), since freewheeling currents from L_r and L_o flow through Q3 in opposite directions.

Fig. 4C (Time period C): Q1 and Q3 are OFF, and Q2 is ON. Freewheeling current from resonant inductor L_r flows into the resonant capacitor C_r and also flows through output inductor L_o into the load. Resonant inductor current I_{L_r} is equal to I_{load} when V_{C_r} is at a maximum. When resonant inductor current I_{L_r} is below I_{load} , resonant capacitor is providing power to the load and output inductor L_o . The current through the resonant inductor L_r decreases rapidly as it is discharged. Resonant inductor current is approximately zero (or slightly negative) at transition T4.

Fig. 4D (Time period D): Q1 is ON, and Q2 and Q3 are OFF. Resonant capacitor C_r continues discharging through the load and through the resonant inductor L_r . Most current from the resonant capacitor C_r flows to the load. A small amount of current from C_r flows through the resonant inductor and into V_{in} , the power source. This results in a small, negative resonant inductor current during period D.

It is noted in the invention that the time periods C and D (the OFF time of switch Q3) preferably have a combined duration of approximately $\frac{3}{2}\pi\sqrt{LC}$, where L is the inductance of the resonant inductor L_r and C is the capacitance of the resonant capacitor C_r . Hence, for a given circuit with fixed values of L and C, the duration of the combined periods C and D is fixed. Fixing the duration of the combined C and D time periods assures that the voltage on the capacitor is zero, or near-zero when synchronous switch Q3 is turned on (i.e. switch Q3 has zero voltage switching, or ZVS).

Exemplary values for the capacitance of the resonant capacitor C_r can be 0.01-1 microFarad. Exemplary values for the inductance of the resonant inductor L_r can be 1-100 nanoHenries. Typical values can be about 0.1 μF and 20 nH for operation at about 1 Mhz. Also, it is noted that resonant inductor L_r should have an inductance that is much less (e.g. less than 1/10) than the value of the output inductor L_o .

The output power can be controlled in the invention by changing the turn-on time of Q3 relative to the turn-off time of Q1 (i.e. changing the duration of period A, when both Q1 and Q3 are ON). Specifically, the output power is increased as the duration of time period A is increased. However, since the duration of time periods C+D is fixed at $\frac{3}{2}\pi\sqrt{LC}$ for a given

circuit, the output power should be adjusted by phase shifting the control of Q3 relative to Q1 and Q2. In other words, power output should be controlled in a given circuit by delaying transitions T1 and T3 by the same amount. This will keep unchanged the sum of the durations of time periods C and D.

5 The ratio of output voltage (V_o) to input voltage (V_{in}) can be adjusted in the invention by varying the combined duration of time periods A and D. Increasing the combined duration A+D will increase the ratio of V_o/V_{in} . For a fixed input voltage, output voltage can be increased by increasing the combined duration of periods A and D.

10 Also, it is significant in the invention that all switches Q1 Q2 Q3 have zero voltage switching (ZVS), or near-ZVS, at turn-on. For Q1, ZVS is provided because the resonant capacitor C_r provides reverse current direction through L_r and Q1 before Q1 is turned on and while Q1 is being turned on. For Q2, ZVS is provided because the body diode of Q2 conducts during the dead time associated with transition T2. For Q3, ZVS is provided because Q3 is turned on when the capacitor is completely discharged, or nearly so. Hence, the present
15 invention provides ZVS for all the switches, and this feature helps to increase efficiency, maximum operating frequency, and reliability.

 Also, switches Q2 and Q3 experience near-zero current (zero-current switching, or ZCS) at turn-off. Switch Q2 experiences near-ZCS since Q2 is turned off at transition T4. Q3 experiences near-ZCS since it is turned off at or close to the time when the current through
20 resonant inductor L_r and output inductor L_o is equal (see transition T3 in Fig. 3.). Switch Q1, however, has a high current at turnoff (transition T2), and so experiences hard switching at turn-off.

 Accurately ZCS can be difficult to achieve in the invention because it requires precise timing control that may not be available. However, in the present invention switches Q2 Q3
25 have very low currents at switch turn-off compared to the prior art. For example, the current at turnoff of switches Q2 and Q3 can be about 5-20% of the output current I_o . So, although the present invention may not provide exactly zero current at turnoff for switches Q2 and Q3, the turnoff current is low enough to provide the benefits of ZCS.

 Compared to the prior art DC-DC buck converters, the ZVS (for switches Q1 Q2 Q3)
30 and near-ZCS condition (for switches Q2 and Q3) provides increased efficiency and improved

reliability for the present quasi-resonant buck converter. ZVS and ZCS are also known in the art as “soft switching”. The switching loss for the present quasi-resonant buck converter is much less than the switching loss in prior art, hard-switched buck converters. In addition, the body diode loss of the synchronous rectifier switch Q3 has been eliminated.

Fig. 5 shows a second embodiment according to the present invention. Specifically, the second embodiment is a quasi-resonant tap-buck converter. The quasi-resonant tap-buck converter has the top switch Q1, auxiliary switch Q2, synchronous switch Q3, resonant capacitor Cr and the resonant inductor Lr. Also, a pair of coupled inductors L1 L2 are connected between the resonant inductor Lr and Load. The coupled inductors L1 L2 are preferably coupled by a magnetic core 24 (e.g. made of ferrite). A clamping capacitor Cc is connected between the auxiliary switch Q2 and the connection point 20. The synchronous switch Q3 and resonant capacitor Cr are connected to Gnd and to a midpoint 28 between the coupled inductors L1 L2. Also, an output capacitor Co is provided in parallel with the Load.

The coupled inductors L1 L2 have a parallel polarity, indicated by the black dots. That is, ‘parallel polarity’ means that black dots 26 are both on the same side (left side in Fig. 5) of the inductors L1 L2. This polarity relationship between L1 and L2 tends to reduce the output voltage, which is desirable in a large voltage step-down application. For example, if the primary/secondary ($N_p:N_s$) turns ratio is 1:1, then the output voltage will be reduced by about 50%. A 1:1 turns ratio will allow the top switch Q1 to operate with 2-fold greater duty cycle than otherwise possible. This is beneficial because a greater duty cycle for Q1 tends to reduce the switching losses and increase power efficiency.

The $N_p:N_s$ turns ratio of the coupled inductors can be varied widely. For example, the turns ratio can be 5:1 or 1:5, or anything in between. A high turns ratio (e.g. 2:1, 3:1) tends to provide a low output voltage. Hence, in order to provide a low output voltage and high duty cycle for Q1, the turns ratio is preferably 1:1 or higher (e.g. 2:1 or 3:1).

The coupled inductors should also have a small magnetizing inductance. This can be provided by an airgap in the magnetic core 24. Also, the leakage inductance of the coupled inductors should be as small as possible.

The clamping capacitor Cc functions as a voltage clamp, and has a relatively constant voltage during operation (voltage polarity indicated in Fig. 5 for the case of a positive input

voltage). The clamping capacitor should therefore have as large a capacitance as possible. For example, the clamping capacitor can have a capacitance value in the range of 0.1-100 μF .

Fig. 6 shows a timing diagram for operating the tap-buck converter of Fig. 5. One full cycle is divided into time periods A, B, C and D. The operation of switches Q1 Q2 and Q3 is a little different compared to the quasi-resonant buck of Fig. 2. As before, however, a short dead time is provided at transitions T2 and T4 so that Q1 and Q2 are never ON at the same time. Also shown in Fig. 6 are the current through the resonant inductor Lr (I_{Lr}), the voltage across the resonant capacitor Cr (V_{Cr}), and the current through the clamping capacitor Cc (I_{Cc}). Also indicated in Fig. 6 at horizontal line 30 is the quantity

$$I_o \times \left(\frac{V_o \times N_p + N_s \times V_{in}}{V_{in}} \right) \times \frac{1}{N_p + N_s}, \text{ which has units of current. This quantity of current is}$$

important in the quasi-resonant tap-buck circuit in that it indicates when synchronous switch Q3 should be turned OFF. Specifically, when the current through Lr is equal to the above equation, the combined current through Cr and Q3 is equal to zero. This aspect is explained in detail below.

Figs. 7A-7D illustrate circuit conditions during time periods A-D, respectively. Figs. 7A-7D are explained below. Arrows in the circuit illustrations indicate the direction of current flow.

Fig. 7A (Time period A) Switches Q1 and Q3 are ON, and Q2 is OFF. Since both Q1 and Q3 are ON, The entire input voltage V_{in} is applied across resonant inductor Lr and primary inductor L1. The current through the resonant inductor Lr and primary inductor L1 rises linearly, as seen in Fig. 6. The current represents stored energy in the resonant inductor Lr. Output voltage is applied across the secondary winding L2.

Figs. 7B1 and 7B2 (Time periods B1 and B2) Q1 is ON, Q2 and Q3 are OFF. When Q3 is turned OFF, current from primary inductor L1 and resonant inductor Lr begins to charge the resonant capacitor Cr. Preferably, Q3 is turned OFF when current through primary inductor L1 is equal to, or slightly higher than the current level illustrated by line 30 in Fig. 6 and expressed in the equation above. During time period B2 (Fig. 7B2), capacitor Cr begins to discharge through L2 and the load.

Fig. 7C (Time period C) Q2 is ON, and Q1 and Q3 are OFF. Capacitor Cr continues to discharge, and provides energy to the load and to clamping capacitor Cc as it discharges. This causes a current pulse through the clamping capacitor.

Fig. 7D (Time period D) Q2 and Q3 are ON, and Q1 is OFF. Synchronous switch Q3 is turned ON when voltage on the resonant capacitor Cr reaches zero. Voltage on the clamping capacitor causes a reverse current flow through the resonant inductor Lr. Fig. 7D illustrates the current flow in the latter portion of time period D, after current flow through Cc has reversed.

It is noted that the combined duration of time periods B and C (equal to the OFF time of the synchronous switch Q3) is preferably approximately $\frac{3}{2}\pi\sqrt{(L+L_k)C}$, where L is the inductance of the resonant inductor Lr, L_k is the leakage inductance of primary winding L1, and C is the capacitance of the resonant capacitor Cr. Preferably, the leakage inductance L_k is as small as possible. Hence, for a given circuit with fixed values of L, L_k , and C, the duration of the combined periods B and C is fixed. Fixing the duration of the combined B and C time periods assures that the voltage on the resonant capacitor is zero, or near-zero when synchronous switch Q3 is turned on (i.e. switch Q3 has zero voltage switching, or ZVS).

In the resonant tap-buck converter of Fig. 5, ZVS and near-ZCS are provided at turn on and turn off for all switches Q1 Q2 Q3 in a manner similar to the device of Fig. 2. Current through Q1 at turn off is very small.

The output power can be controlled in the circuit of Fig. 5 by changing the time of transition T4 (Q2 turnoff and Q1 turn on) relative to the time of transition T1 (i.e. changing the duration of period A, when both Q1 and Q3 are ON). Specifically, the output power is increased as the duration of time period A is increased.

The ratio of output voltage to input voltage (V_o/V_{in}) can be adjusted in the tap-buck embodiment by varying the combined duration of time periods A and B. Increasing the combined duration A+B will increase the ratio of V_o/V_{in} . For a fixed input voltage, output voltage can be increased by increasing the combined duration of periods A and B.

The quasi-resonant tap-buck converter of Fig. 5 can have a higher duty cycle than the quasi-resonant buck converter of Fig. 2. As a result, the quasi-resonant tap-buck will tend to

have a higher efficiency (from reduced conduction loss and lower switching loss), and can have a higher operating frequency. The higher duty cycle is provided by the coupled inductors L1 L2, which tend to reduce the output voltage.

Fig. 8 shows an embodiment of the invention providing isolation between the input and output. Like the resonant tap-buck embodiment of Fig. 5, the device of Fig. 8 has the connection point 20, the top switch Q1, the auxiliary switch Q2, the clamping capacitor Cc, the resonant inductor Lr, the synchronous switch Q3, and the resonant capacitor Cr. The circuit also has an isolation transformer 40 connected between the resonant inductor, and the synchronous switch Q3 and resonant capacitor Cr. The isolation transformer 40 has a primary winding 42 and a secondary winding 44. The primary winding 42 is connected between the resonant inductor Lr and the return potential Gnd. The secondary winding 44 is connected in series with the synchronous switch Q3 and resonant capacitor Cr. The Load is also connected in series with the secondary winding and synchronous switch Q3, and the output capacitor Co is connected in parallel with the Load.

Dots 46 illustrate the preferred polarity of the transformer windings. If the polarity of the transformed is reversed, then the polarity of the synchronous switch should also be reversed.

The transformer can be a step-up or step-down transformer. In most applications, the transformer will be a step-down transformer, and will thereby serve to provide low-voltage, high current output power. The transformer can have a primary:secondary turns ratio in a wide range, for example in the range of 5:1 to 1:5.

Fig. 9 shows a timing diagram illustrating the operation of the isolated circuit of Fig. 8. The operation of the isolated circuit is very similar to the resonant tap-buck circuit of Fig. 5. For example the control of switches Q1 Q2 and Q3 is the same. However, there are at least a few key differences between the resonant tap buck of Fig. 5, and the transformer-isolated circuit of Fig. 8: (1) at T1, synchronous switch Q3 is turned OFF when the resonant inductor Lr current is approximately equal to the magnetization current Lm indicated at 48, instead of the current level indicated at 30 (2) the combined duration of time periods B+C is dependent upon the transformer turns ratio.

Figs.10A-10D illustrate circuit conditions during time periods A-D, respectively. Figs. 10A-10D are explained below. For brevity, the optional output capacitor Co is not shown. Arrows in the circuit illustrations indicate the direction of current flow.

Fig. 10A (time period A) Switches Q1 and Q3 are ON, switch Q2 is OFF. The voltage difference between Vin and the output voltage is applied across resonant inductor Lr. Current through the resonant inductor Lr and transformer primary 42 rises linearly, thereby storing energy in the resonant inductor Lr. The rising current also induces current in the transformer secondary 44, which is provided to the Load. The duration of time period A, and the amount of energy stored in resonant inductor Lr, determines the output power.

Fig. 10B1 (time period B1) Switch Q1 is ON, and switches Q2 and Q3 are OFF. The resonant capacitor Cr is charged by the difference in current between resonant inductor Lr and magnetizing current Im of the transformer. Preferably, synchronous switch Q3 is turned OFF when the current through Lr is equal to, or slightly greater than the magnetizing current Im, indicated by horizontal line 48 in Fig. 9.

Fig. 10B2 (time period B2) Switch Q1 is ON, and switches Q2 and Q3 are OFF. Voltage on the resonant capacitor Cr peaks as resonant inductor current falls below the magnetizing current Im. After resonant inductor current falls below Im, resonant capacitor begins to discharge through the secondary winding 44 to the Load.

Fig. 10C (time period C) Switch Q2 is ON, and switches Q1 and Q3 are OFF. Resonant capacitor continues to discharge, and provides energy to the load and to clamping capacitor Cc as it discharges. This causes a current pulse through the clamping capacitor.

Fig. 10D (time period D) Switches Q2 and Q3 are ON, and switch Q1 is OFF. Synchronous switch Q3 is turned ON when resonant capacitor voltage VCr reaches zero. Voltage on the clamping capacitor causes a reverse current flow through the resonant inductor Lr. Fig. 10D illustrates the current flow in the latter portion of time period D, after current flow through Cc has reversed.

The magnetizing current Im in general is given by $I_o \left(\frac{V_o}{V_{in}} + \frac{N_s}{N_p} \right)$, where Io is the output current (Load current), Vo is the output voltage, Vin is the input voltage, Ns is the

numbers of turns in the secondary winding 44, and N_p is the number of turns in the primary winding 42.

It is noted that the combined duration of time periods B and C (equal to the OFF time of the synchronous switch Q3) is preferably approximately $\frac{3}{2} \pi \frac{N_s}{N_p} \sqrt{(L + L_k)C}$ where L is the

5 inductance of the resonant inductor L_r , L_k is the leakage inductance of the transformer, C is the capacitance of the resonant capacitor C_r , N_s is the number of turns in the secondary winding 44, and N_p is the number of turns in the primary winding 42. Hence, for a given circuit with fixed values of L, L_k , N_s , N_p and C, the duration of the combined periods B and C is fixed. Fixing the duration of the combined B and C time periods assures that the voltage on
10 the resonant capacitor is zero, or near-zero when synchronous switch Q3 is turned on (i.e. switch Q3 has zero voltage switching, or ZVS). Preferably, the leakage inductance L_k is as small as possible.

In the transformer-isolated embodiment of Fig. 8, all switches Q1 Q2 and A3 have ZVS and near-ZCS. That is, switch current is zero or nearly zero at turn-off, and switch
15 voltage is zero or nearly zero at turn-on.

It is noted that the voltage on the clamping capacitor C_c is nearly constant. As in the case of the quasi-resonant tap-buck, the clamping capacitor should have as large a capacitance as practical.

The output power can be controlled in the circuit of Fig. 8 by changing the time of
20 transition T4 (Q2 turnoff and Q1 turn on) relative to the time of transition T1 (i.e. changing the duration of period A, when both Q1 and Q3 are ON). Specifically, the output power is increased as the duration of time period A is increased.

The ratio of output voltage to input voltage (V_o/V_{in}) can be adjusted in the transformer-isolated embodiment by varying the combined duration of time periods A and B.
25 Increasing the combined duration A+B will increase the ratio of V_o/V_{in} . For a fixed input voltage, output voltage can be increased by increasing the combined duration of periods A and B.

The transformer-isolated circuit of Fig. 8 can have a relatively high duty cycle compared to the quasi-resonant buck circuit of Fig. 2 if the transformer has a turns ratio of

greater than 1 (i.e. if the primary winding 42 has more turns than the secondary winding 44). This is because such a transformer will tend to reduce the output voltage. For example, if the primary/secondary ($N_p:N_s$) turns ratio is 2:1, then the output voltage will be reduced by about 50%. A 2:1 turns ratio will allow the top switch Q1 to operate with 2-fold greater duty cycle than otherwise possible. This is beneficial because a greater duty cycle for Q1 tends to reduce the switching losses and increase power efficiency. The $N_p:N_s$ turns ratio of the transformer can be varied widely. A high turns ratio (e.g. 6:1, 8:1) tends to provide a low output voltage. Hence, in order to provide a low output voltage with 48V input, and high duty cycle for Q1, the turns ratio is preferably 6:1 or higher (e.g. 8:1 or 10:1).

It will be clear to one skilled in the art that the above embodiment may be altered in many ways without departing from the scope of the invention. Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents.